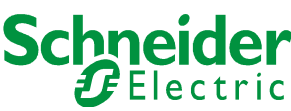


Release history for PM5330

Release Version	Date	OS Version	RS version	Language Version
1.50	14/05/2015	1.5.0	1.0.6	2.0.0
1.37	4/11/2014	1.3.7	1.0.6	2.0.0
1.12	12/03/2013	1.1.2	1.0.6	1.0.3
1.11	29/08/2013	1.1.1	1.0.5	1.0.3
1.00	18/06/2013	1.0.0	1.0.4	1.0.2

Revision	Changes Since Version	Change Details
1.50	1.37	Enhancements <ul style="list-style-type: none"> 4 additional communication registers to provide PF value in IEC and Lag/lead format. These are 2 float 32 registers (3192, 3194) and 2 INT16 registers (3196, 3197) 10 additional logs for Firmware down load Evenly spaced pulses similar to optical pulse output implemented for Digital output Fixes <ul style="list-style-type: none"> Individual harmonic values not accessible through communication fixed Spurious neutral current while phases carry balanced currents fixed Demand Fix to Correct the behavior in Command Sync and Clock Sync Mode DI/DO/Relay counter value not reset to zero by Global reset through HMI fixed
1.37	1.11	Enhancement <ul style="list-style-type: none"> Added Float 32 energy registers to support both INT64 and Float 32 energy registers Added QR code Functionality Fixes <ul style="list-style-type: none"> Fix issue : Multi tariff energy not retaining value on power cycle while Multi tariff in Input mode Fix issue : RTC day roll over not in sync with 24 hours. Fix issue : After data log roll over value only partial records are retrievable
1.12	1.11	Fix : <ul style="list-style-type: none"> Fix issue :DLF upgrade errors at 38400 baud rate
1.11	1.00	Note : 1.0.0 can't be field upgraded to 1.1.1 Enhancement <ul style="list-style-type: none"> common language file for all models 61557-12 compliance Support added for new display (Tianma) Fixes



PM5330 FW Releases

		<ul style="list-style-type: none">Default settings for Digital Output is Initialized to Zero
1.00	None	First Release